FIG.1

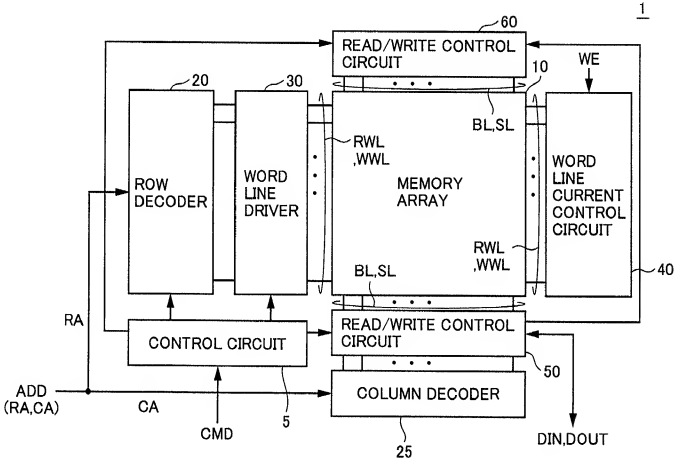

FIG.2

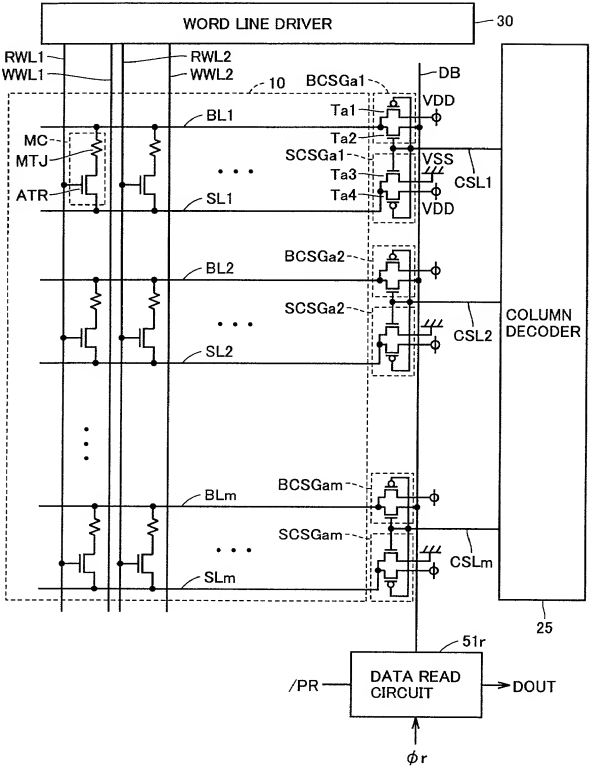
WORD LINE DRIVER
30
RWL1
WWL1
RWL2
WWL2
10
BCSGa1
DB
VDD
Ta1
BL1
Ta2
MC
MTJ
SCSGa1
VSS
Ta3
CSL1
ATR
SL1
Ta4
VDD
BCSGa2
BL2
SCSGa2
CSL2
COLUMN DECODER
SL2
BCSGam
BLm
SCSGam
CSLm
SLm
25
51r
/PR
DATA READ CIRCUIT
DOUT
φr

FIG.3

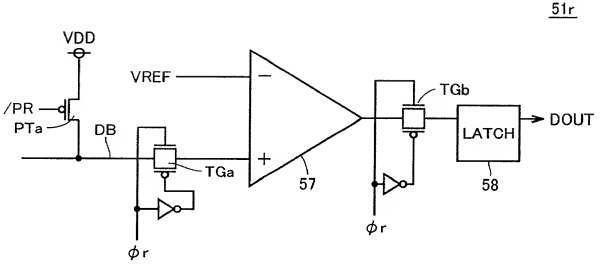
51r
VDD
VREF
/PR
PTa
DB
TGa
57
TGb
LATCH
58
DOUT
φr
φr

FIG.4

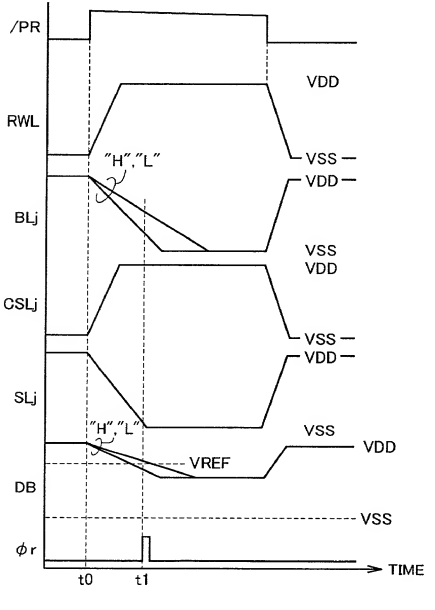
/PR
RWL
VDD
VSS
"H","L"
VDD
BLj
VSS
VDD
CSLj
VSS
VDD
SLj
"H","L"
VSS
VDD
VREF
DB
VSS
φr
TIME
t0
t1

FIG.5

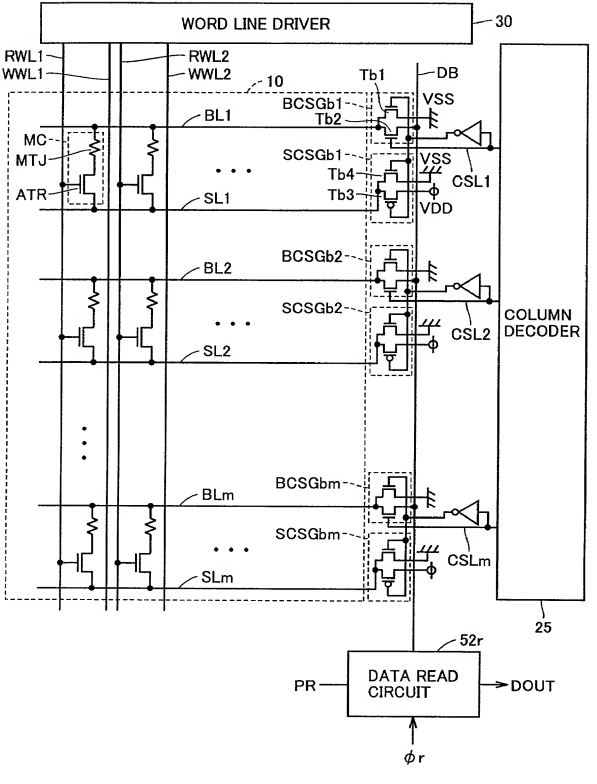
WORD LINE DRIVER
30
RWL1
WWL1
RWL2
WWL2
10
Tb1
DB
BCSGb1
Tb2
VSS
BL1
MC
MTJ
ATR
SL1
SCSGb1
Tb4
Tb3
VSS
VDD
CSL1
BCSGb2
BL2
SCSGb2
SL2
CSL2
COLUMN DECODER
BCSGbm
BLm
SCSGbm
SLm
CSLm
25
52r
PR
DATA READ CIRCUIT
DOUT
φr

FIG.6

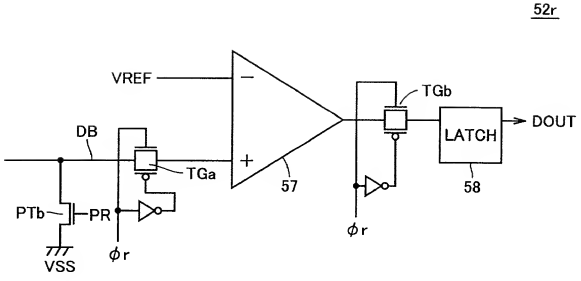
52r
VREF
DB
TGa
PTb
PR
VSS
ϕr
57
TGb
LATCH
58
DOUT

FIG.7

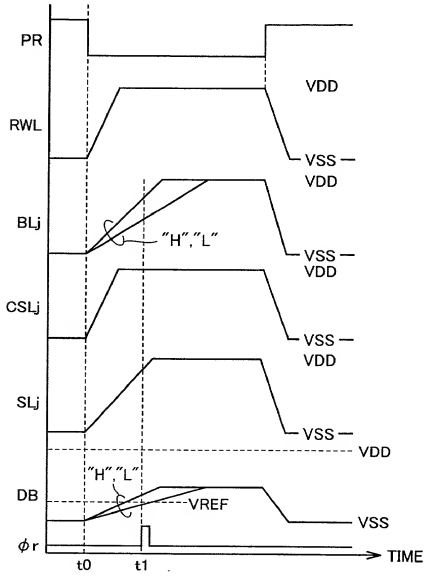
PR
RWL
BLj
CSLj
SLj
DB
ϕr
VDD
VSS
"H","L"
VREF
t0
t1
TIME

FIG.8

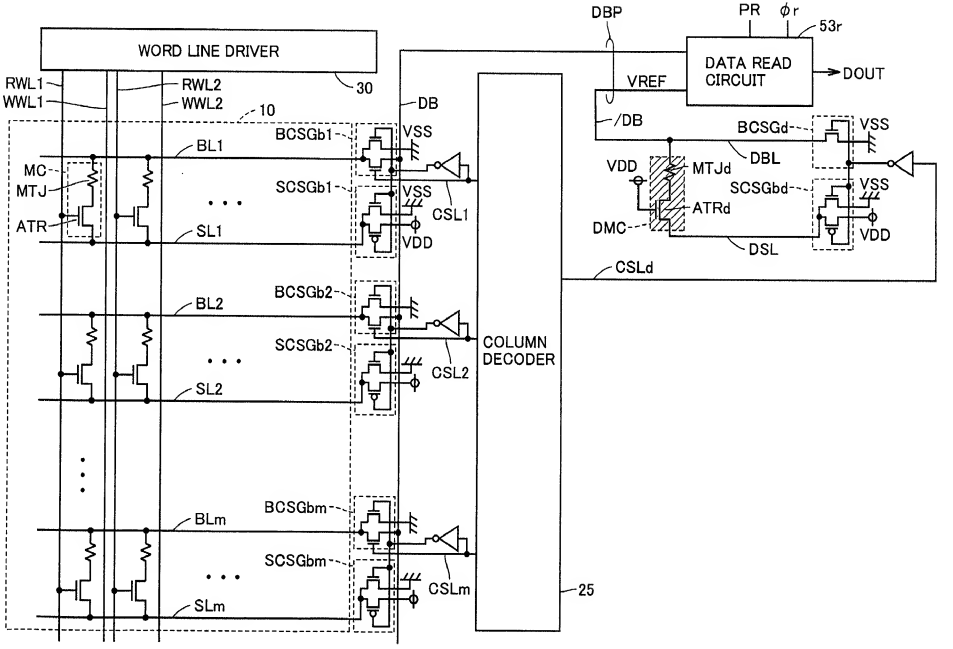
WORD LINE DRIVER
30
RWL1
WWL1
RWL2
WWL2
10
DB
DBP
PR
φr
53r
DATA READ CIRCUIT
DOUT
VREF
/DB
BCSGb1
BL1
MC
MTJ
ATR
SCSGb1
SL1
VSS
CSL1
VDD
BCSGb2
BL2
SCSGb2
SL2
CSL2
COLUMN DECODER
BLm
BCSGbm
SCSGbm
SLm
CSLm
25
BCSGd
DBL
VDD
MTJd
SCSGbd
ATRd
DMC
DSL
CSLd

FIG.9

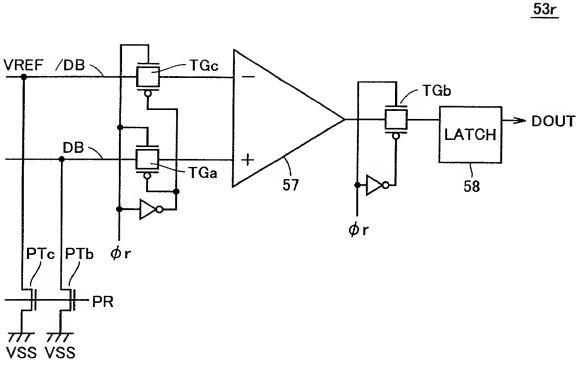
53r
VREF
/DB
TGc
DB
TGa
PTc
PTb
ϕr
PR
VSS
VSS
57
TGb
LATCH
DOUT
58
ϕr

FIG.10

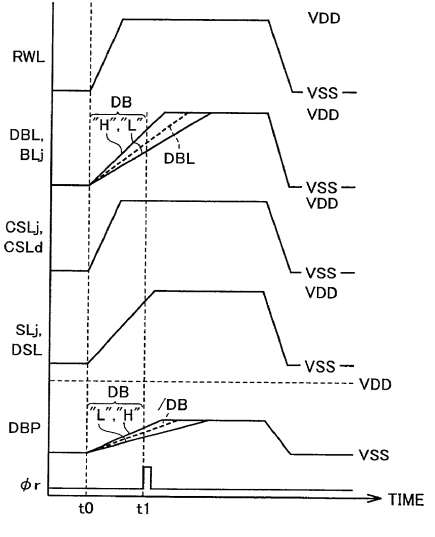
RWL
VDD
VSS
DB
"H","L"
DBL,
BLj
VDD
DBL
VSS
VDD
CSLj,
CSLd
VSS
VDD
SLj,
DSL
VSS
VDD
DB
/DB
"L","H"
DBP
VSS
ϕr
t0
t1
TIME

FIG.11

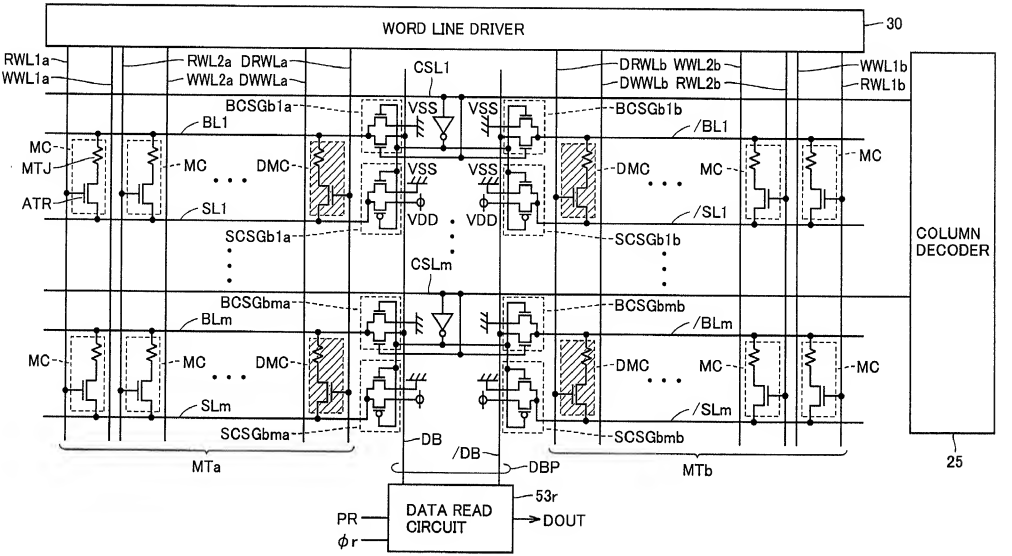
WORD LINE DRIVER
30
RWL1a
WWL1a
RWL2a DRWLa
WWL2a DWWLa
CSL1
DRWLb WWL2b
DWWLb RWL2b
WWL1b
RWL1b
BCSGb1a
BL1
VSS
VSS
BCSGb1b
/BL1
MC
MTJ
ATR
MC
DMC
VSS
VSS
DMC
MC
MC
SL1
VDD
VDD
/SL1
SCSGb1a
SCSGb1b
CSLm
COLUMN DECODER
BCSGbma
BLm
BCSGbmb
/BLm
MC
MC
DMC
DMC
MC
MC
SLm
/SLm
SCSGbma
SCSGbmb
DB
/DB
DBP
MTa
MTb
25
53r
DATA READ CIRCUIT
PR
φr
DOUT

FIG.12

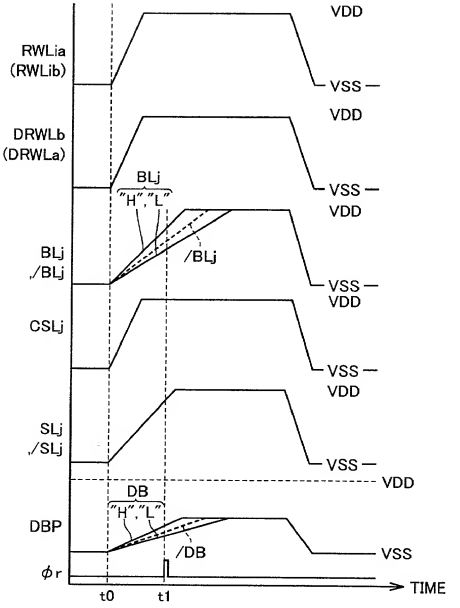
VDD
RWLia
(RWLib)
VSS
VDD
DRWLb
(DRWLa)
BLj
"H","L"
VSS
VDD
BLj
/BLj
/BLj
VSS
VDD
CSLj
VSS
VDD
SLj
/SLj
VSS
VDD
DB
"H","L"
DBP
/DB
VSS
φr
t0
t1
TIME

FIG.13

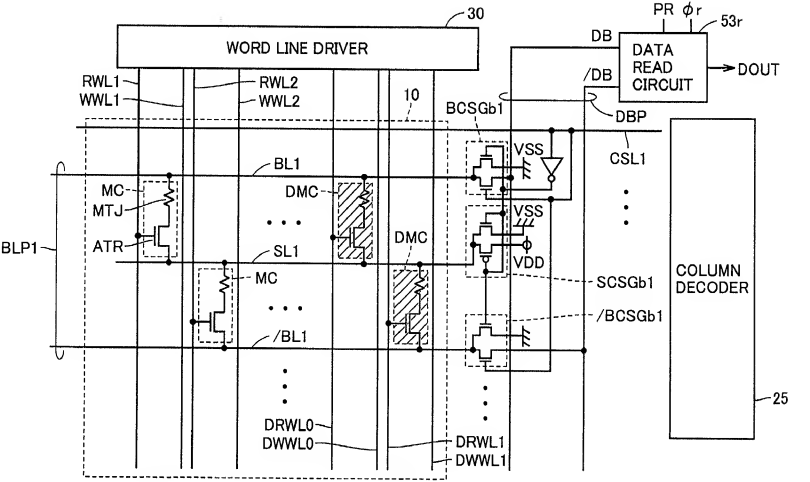
30
WORD LINE DRIVER
PR
φr
53r
DB
/DB
DATA READ CIRCUIT
DOUT
DBP
RWL1
WWL1
RWL2
WWL2
10
BCSGb1
VSS
CSL1
BL1
MC
MTJ
ATR
DMC
VSS
VDD
SL1
BLP1
SCSGb1
/BCSGb1
/BL1
COLUMN DECODER
25
DRWL0
DWWL0
DRWL1
DWWL1

FIG.14

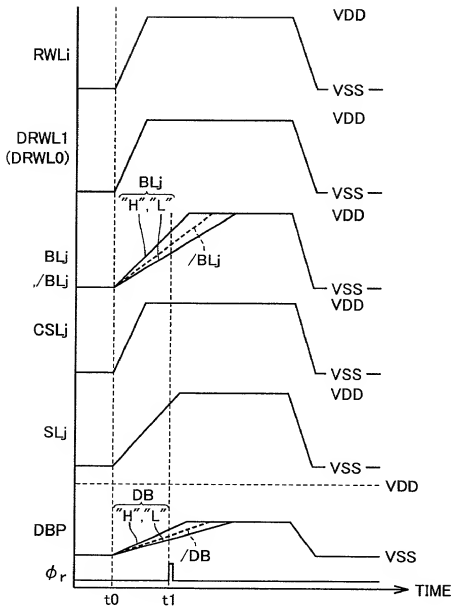
RWLi
VDD
VSS
DRWL1
(DRWL0)
VDD
VSS
BLj
"H", "L"
VDD
BLj
/BLj
/BLj
VSS
VDD
CSLj
VSS
VDD
SLj
VSS
VDD
DB
"H", "L"
DBP
/DB
VSS
ϕ_r
t0
t1
TIME

FIG.15

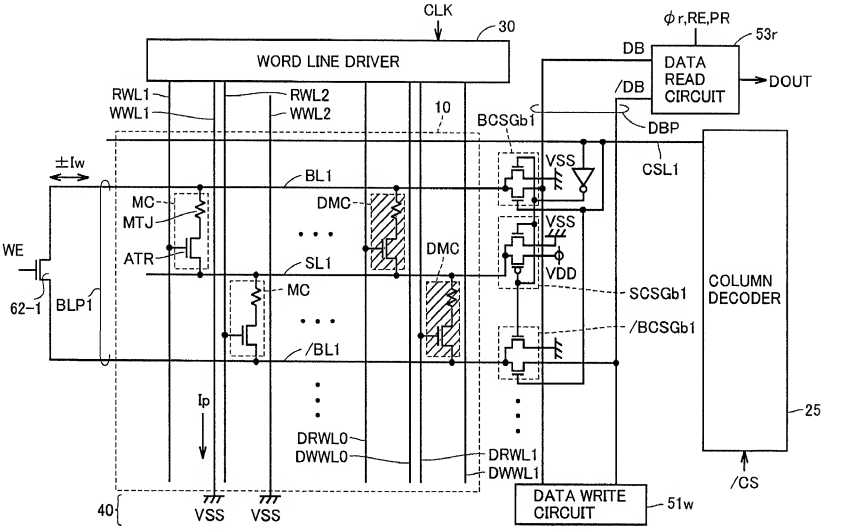
CLK
30
WORD LINE DRIVER
φr,RE,PR
53r
DB
DATA READ CIRCUIT
DOUT
/DB
DBP
RWL1
WWL1
RWL2
WWL2
10
BCSGb1
VSS
CSL1
±Iw
BL1
MC
MTJ
ATR
DMC
SL1
WE
62-1
BLP1
/BL1
SCSGb1
/BCSGb1
COLUMN DECODER
25
Ip
DRWL0
DWWL0
DRWL1
DWWL1
/CS
40
VSS
VSS
DATA WRITE CIRCUIT
51w

FIG.16

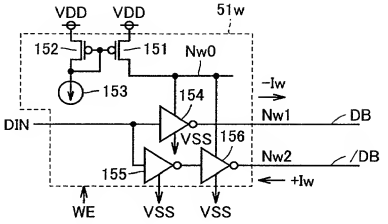

FIG.17

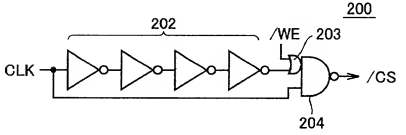

FIG.18

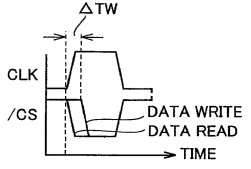

FIG.19

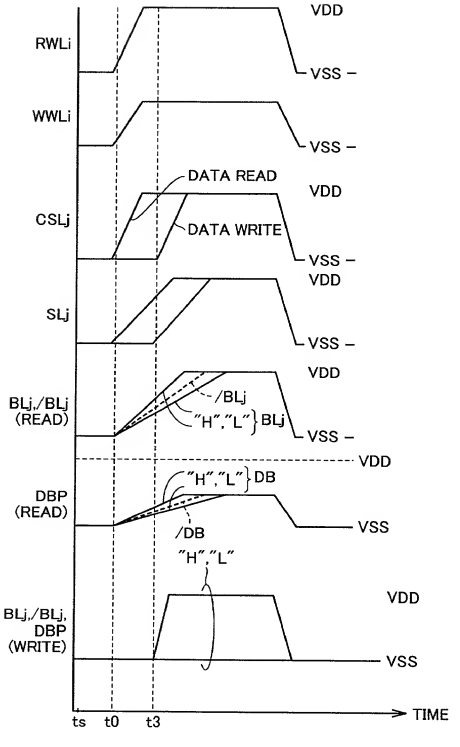
RWLi
VDD
VSS
WWLi
VDD
VSS
DATA READ
CSLj
DATA WRITE
VDD
VSS
SLj
VDD
VSS
BLj,/BLj
(READ)
VDD
/BLj
"H","L"
BLj
VSS
VDD
"H","L"
DB
DBP
(READ)
/DB
VSS
"H","L"
VDD
BLj,/BLj,
DBP
(WRITE)
VSS
TIME
ts
t0
t3

FIG.20

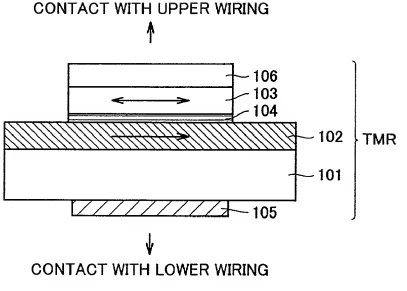
CONTACT WITH UPPER WIRING
106
103
104
102
TMR
101
105
CONTACT WITH LOWER WIRING

FIG.21

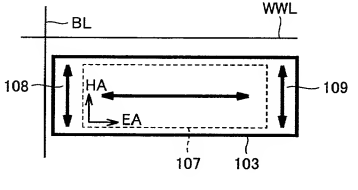
WWL
BL
108
HA
EA
109
107
103

FIG.22

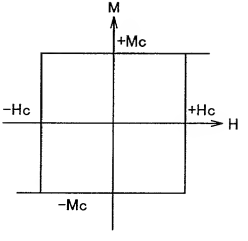

FIG.23

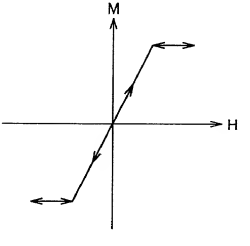

FIG.24A

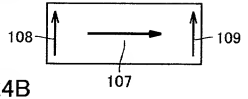

FIG.24B

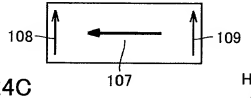

FIG.24C

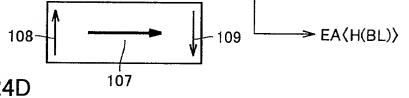

FIG.24D

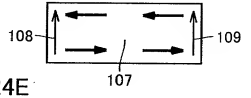

FIG.24E

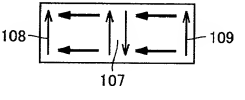

FIG.25

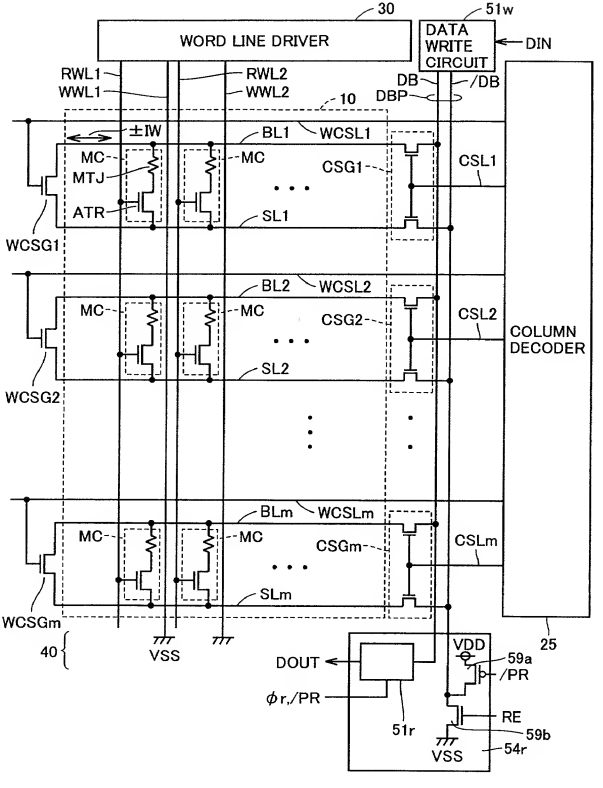
30
51w
WORD LINE DRIVER
DATA WRITE CIRCUIT
DIN
RWL1
WWL1
RWL2
WWL2
10
DB
/DB
DBP
±IW
BL1
WCSL1
MC
MTJ
ATR
CSG1
CSL1
SL1
WCSG1
BL2
WCSL2
CSG2
CSL2
SL2
WCSG2
COLUMN DECODER
BLm
WCSLm
CSGm
CSLm
SLm
WCSGm
40
VSS
DOUT
VDD
59a
/PR
φr,/PR
51r
RE
59b
VSS
54r
25

FIG.26

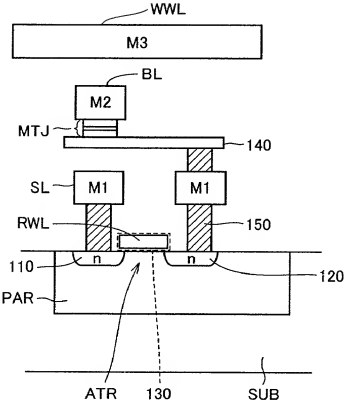

FIG.27

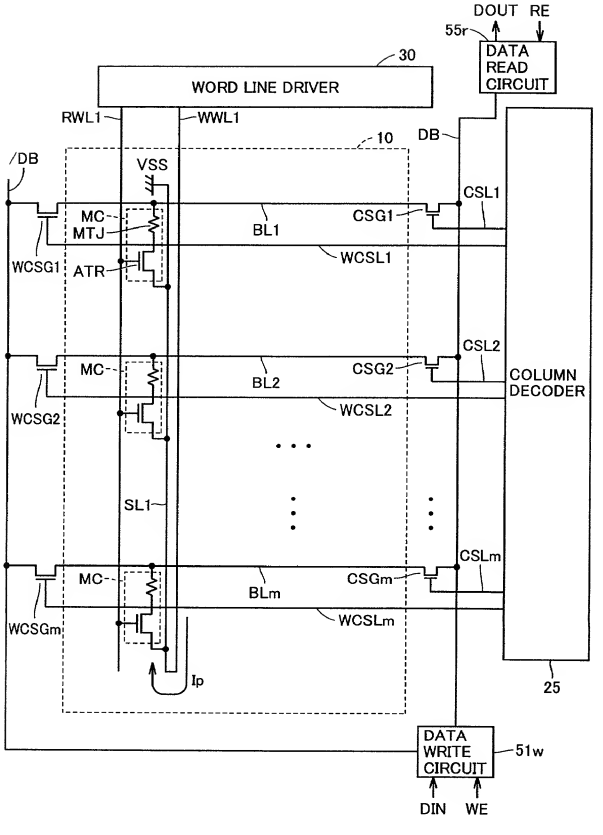
DOUT RE
55r
DATA READ CIRCUIT
30
WORD LINE DRIVER
RWL1
WWL1
10
DB
/DB
VSS
CSL1
MC
MTJ
BL1
CSG1
WCSG1
ATR
WCSL1
CSL2
MC
BL2
CSG2
COLUMN DECODER
WCSG2
WCSL2
SL1
CSLm
MC
BLm
CSGm
WCSGm
WCSLm
Ip
25
DATA WRITE CIRCUIT
51w
DIN
WE

FIG.28

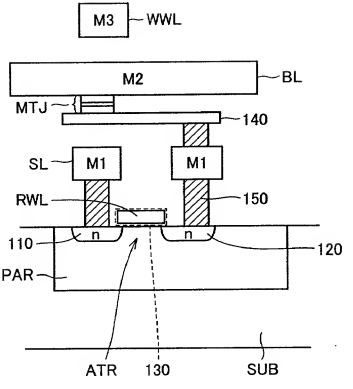
M3
WWL
M2
BL
MTJ
140
SL
M1
M1
RWL
150
110
n
n
120
PAR
ATR
130
SUB

FIG.29

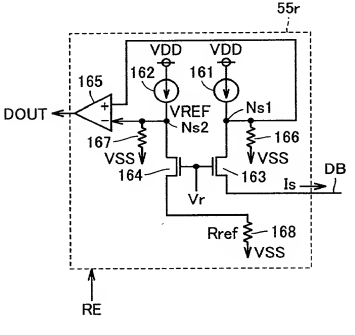
55r
VDD
VDD
162
161
165
DOUT
VREF
Ns1
Ns2
166
167
VSS
VSS
164
163
Is
DB
Vr
Rref
168
VSS
RE

FIG.30

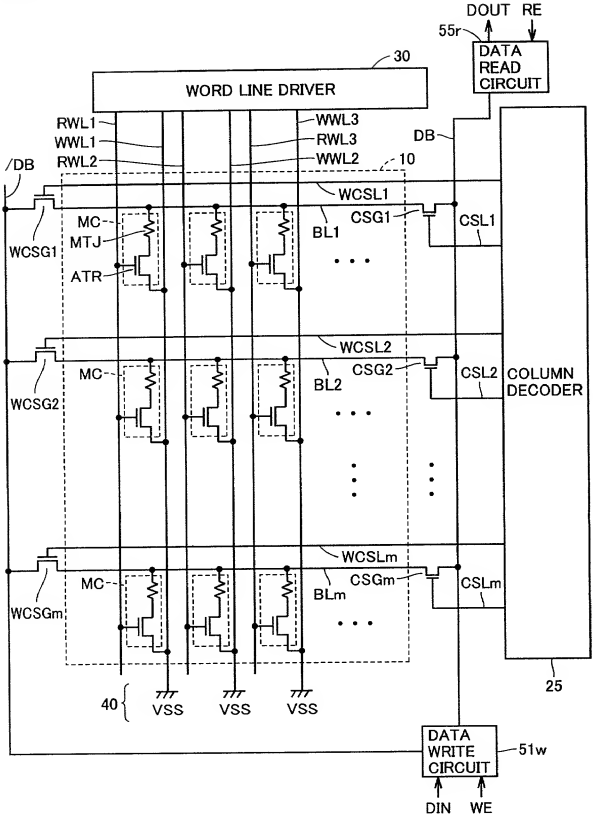
DOUT RE
55r
DATA READ CIRCUIT
30
WORD LINE DRIVER
RWL1
WWL1
RWL2
WWL3
RWL3
WWL2
DB
/DB
10
WCSL1
CSG1
CSL1
MC
MTJ
ATR
WCSG1
BL1
WCSL2
CSG2
CSL2
COLUMN DECODER
WCSG2
BL2
WCSLm
CSGm
CSLm
WCSGm
BLm
25
40
VSS
VSS
VSS
DATA WRITE CIRCUIT
51w
DIN WE

FIG.31

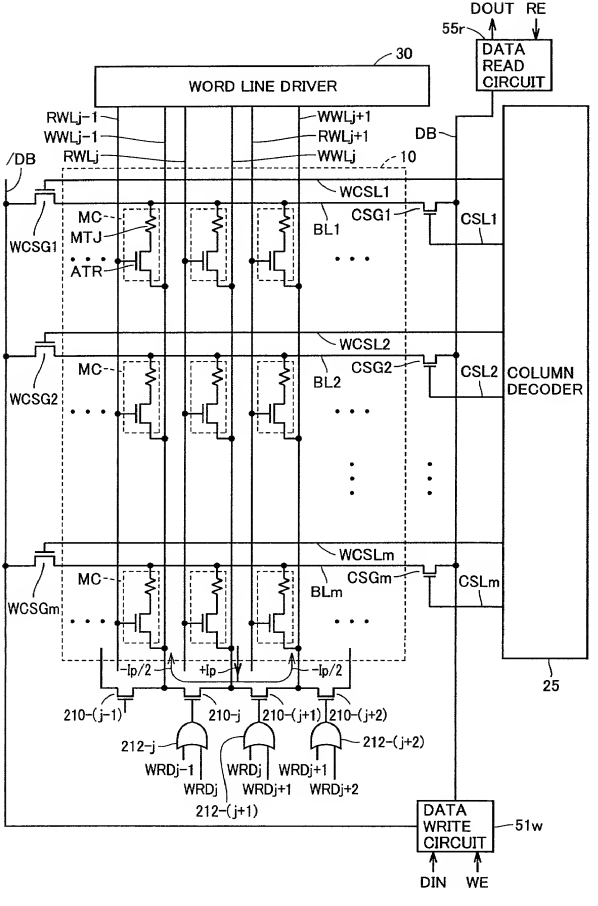
DOUT RE
55r
DATA READ CIRCUIT
30
WORD LINE DRIVER
RWLj-1
WWLj-1
RWLj
WWLj+1
RWLj+1
WWLj
DB
/DB
10
WCSL1
MC
MTJ
ATR
WCSG1
BL1
CSG1
CSL1
WCSL2
WCSG2
BL2
CSG2
CSL2
COLUMN DECODER
WCSLm
WCSGm
BLm
CSGm
CSLm
25
-Ip/2
+Ip
-Ip/2
210-(j-1)
210-j
210-(j+1)
210-(j+2)
212-j
212-(j+2)
WRDj-1
WRDj
WRDj
WRDj+1
WRDj+1
WRDj+2
212-(j+1)
DATA WRITE CIRCUIT
51w
DIN
WE

FIG.32

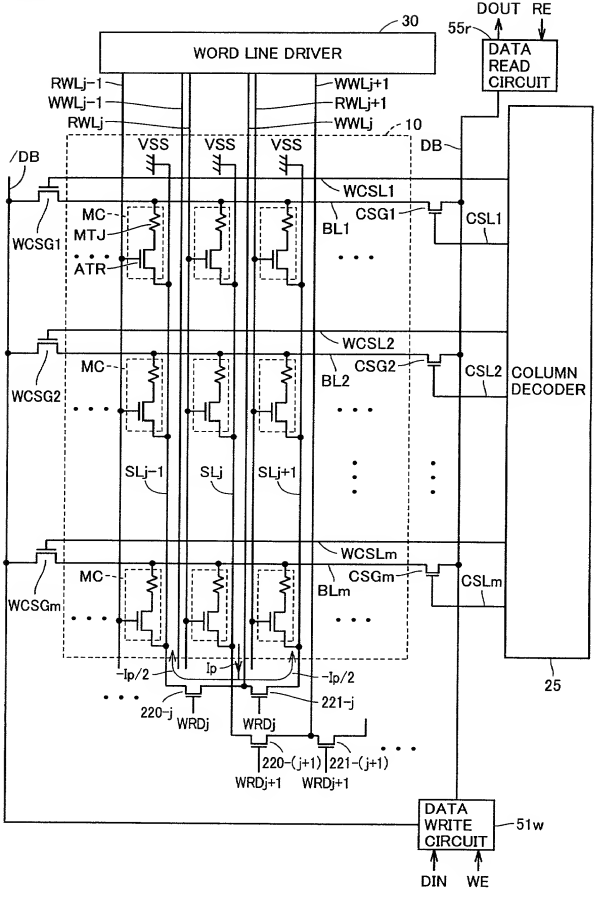
30
WORD LINE DRIVER
DOUT RE
55r
DATA READ CIRCUIT
RWLj-1
WWLj-1
RWLj
WWLj+1
RWLj+1
WWLj
10
/DB
VSS
VSS
VSS
DB
WCSL1
MC
MTJ
ATR
WCSG1
BL1
CSG1
CSL1
WCSL2
WCSG2
BL2
CSG2
CSL2
COLUMN DECODER
SLj-1
SLj
SLj+1
WCSLm
WCSGm
BLm
CSGm
CSLm
-Ip/2
Ip
-Ip/2
221-j
220-j
WRDj
WRDj
220-(j+1)
221-(j+1)
WRDj+1
WRDj+1
25
DATA WRITE CIRCUIT
51w
DIN
WE

FIG.33

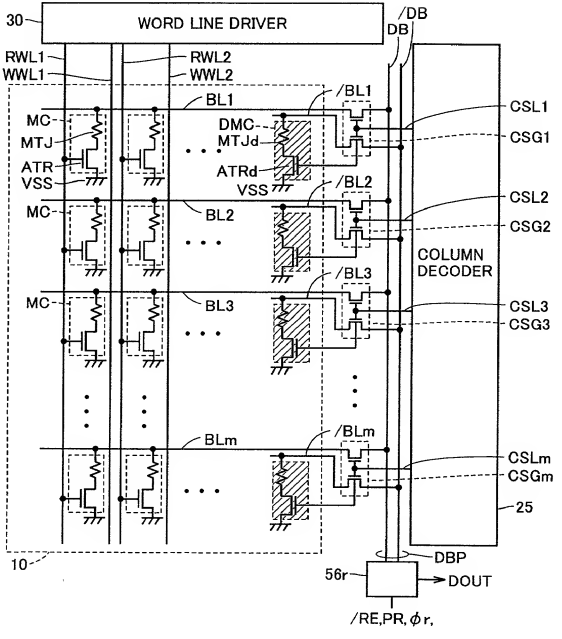
30
WORD LINE DRIVER
/DB
DB
RWL1
WWL1
RWL2
WWL2
BL1
/BL1
CSL1
CSG1
MC
MTJ
ATR
VSS
DMC
MTJd
ATRd
VSS
/BL2
CSL2
CSG2
BL2
COLUMN
DECODER
/BL3
CSL3
CSG3
BL3
BLm
/BLm
CSLm
CSGm
25
10
DBP
56r
DOUT
/RE,PR,φr,

FIG.34

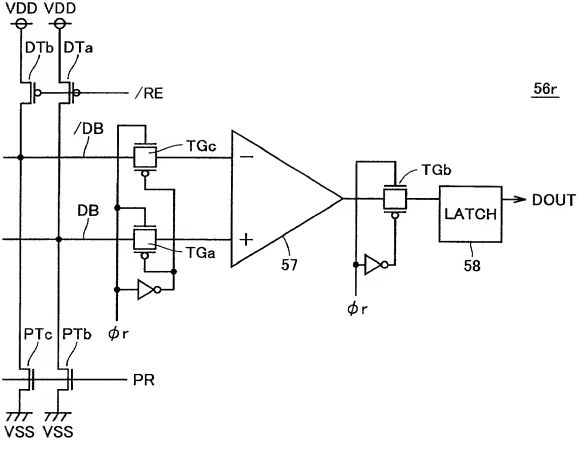
VDD VDD
DTb DTa
/RE
56r
/DB
TGc
DB
TGa
57
TGb
LATCH
DOUT
58
ϕr
ϕr
PTc PTb
PR
VSS VSS

FIG.35

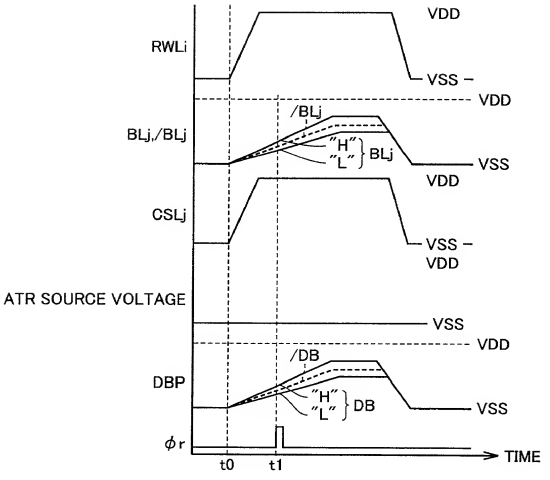
RWLi
VDD
VSS
VDD
/BLj
BLj,/BLj
"H"
"L"
BLj
VSS
VDD
CSLj
VSS
VDD
ATR SOURCE VOLTAGE
VSS
VDD
/DB
DBP
"H"
"L"
DB
VSS
φr
t0
t1
TIME

FIG.36

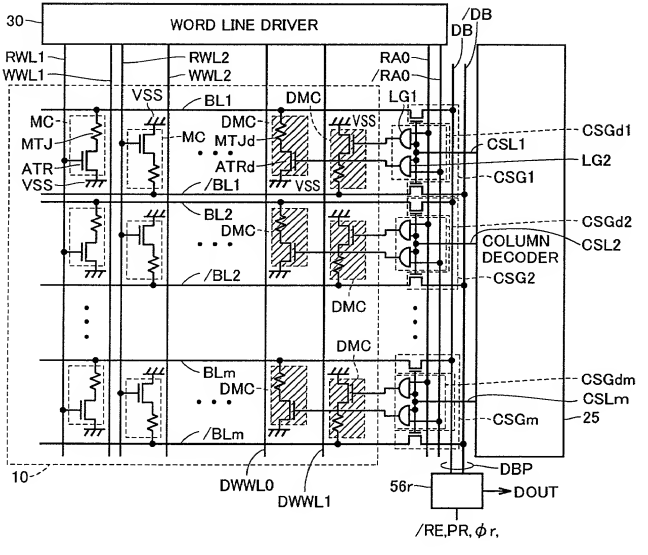
30
WORD LINE DRIVER
/DB
DB
RWL1
WWL1
RWL2
WWL2
RA0
/RA0
VSS
BL1
DMC
LG1
MC
MTJ
ATR
VSS
DMC
MC
MTJd
ATRd
/BL1
VSS
VSS
CSGd1
CSL1
LG2
CSG1
BL2
DMC
/BL2
CSGd2
CSL2
COLUMN
DECODER
CSG2
DMC
DMC
BLm
DMC
/BLm
CSGdm
CSLm
CSGm
25
10
DWWL0
DWWL1
DBP
56r
DOUT
/RE,PR,φr,

FIG.37

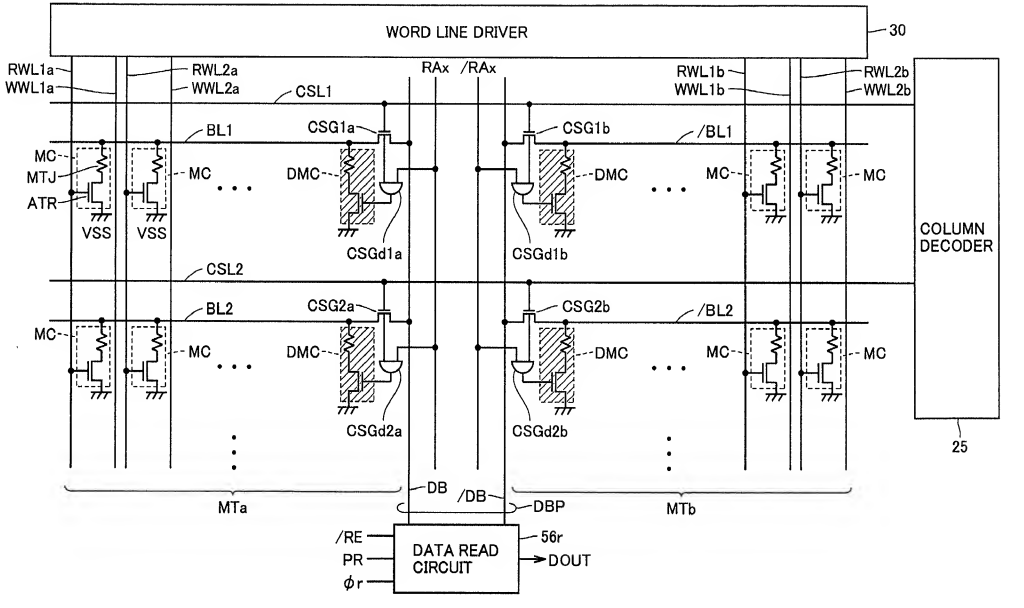
WORD LINE DRIVER
30
RWL1a
WWL1a
RWL2a
WWL2a
CSL1
RAx
/RAx
RWL1b
WWL1b
RWL2b
WWL2b
BL1
CSG1a
CSG1b
/BL1
MC
MTJ
ATR
VSS
DMC
CSGd1a
CSGd1b
COLUMN DECODER
CSL2
BL2
CSG2a
CSG2b
/BL2
CSGd2a
CSGd2b
25
DB
/DB
DBP
MTa
MTb
/RE
PR
φr
DATA READ CIRCUIT
56r
DOUT

FIG.38

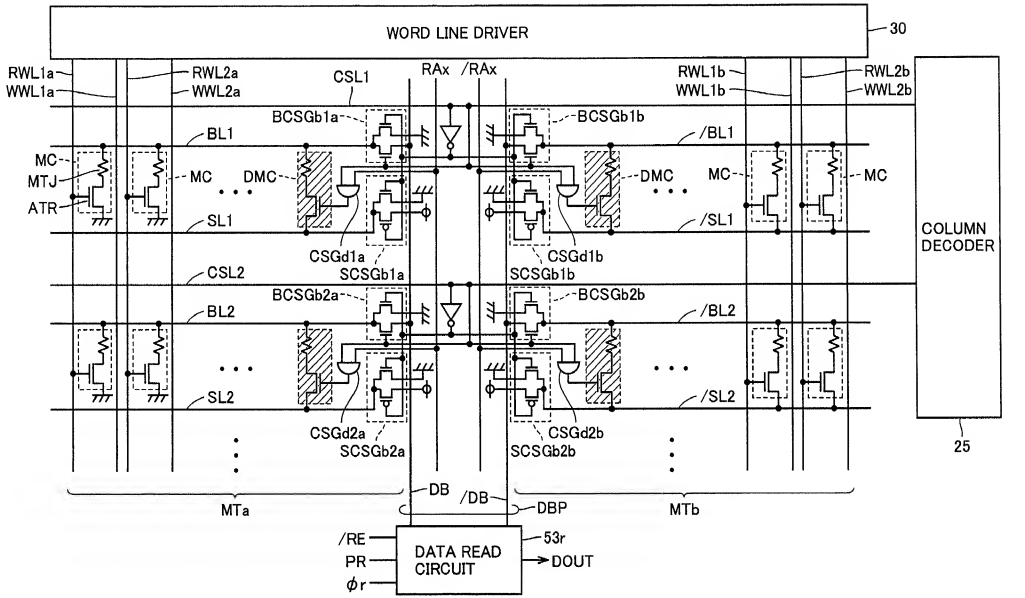

FIG.39 PRIOR ART

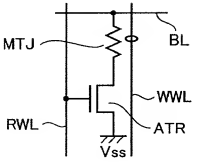

FIG.40 PRIOR ART

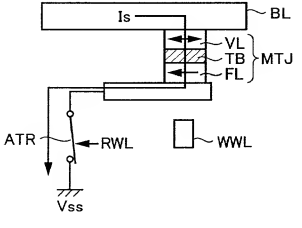

FIG.41 PRIOR ART

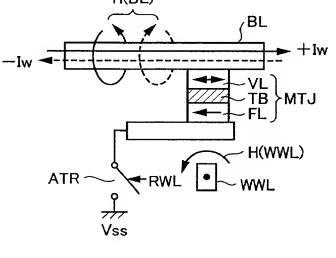

FIG.42 PRIOR ART

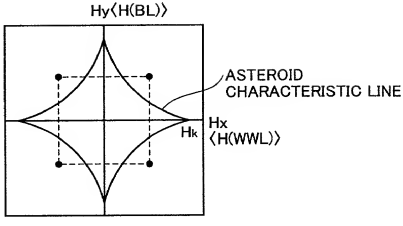

FIG.43 PRIOR ART